SPECIFICATION APPENDIX

The paragraph beginning on line 2 of page 4 has been amended as follows:

One input pair (a_i, b_i) may or may not make a carry request. If two input pairs (a_i, b_i) and (a_j, b_j) are used, two carry requests may occur at the same time. Therefore, it is necessary to arbitrate these two carry requests. It is of note that i and j relate to two adjacent bits (at the first level) or blocks of bits (at subsequent levels) in the calculation, thus if we are arbitrating between carry requests relating to previously arbitrated blocks of 3 bits, then i=j+ 3.

The paragraph beginning on line 15 of page 6 has been amended as follows:

The following equations satisfy Tables 3 and 4:

$V_i = a_ib_i + (a_i + b_i)(a_jb_j + (a_j + b_j)a_k)$ (3)

$V_i = a_ib_i + (a_j + b_i)(a_jb_j + (a_j + b_j)b_k)$

The paragraph beginning on line 18 of page 7 has been amended as follows:

Figure 6 shows the part of the circuit that generates the 31st bit carry. Analogous circuit (interconnections) to those shown in Figures 7 and 8 are used for the other bits of the carry result. Once a carry bit has been determined (i.e. the carry-in and structure [result] results in a generate or a kill, with propagate not being possible at that point), then a single signal wire may be used to pass that result to higher levels.